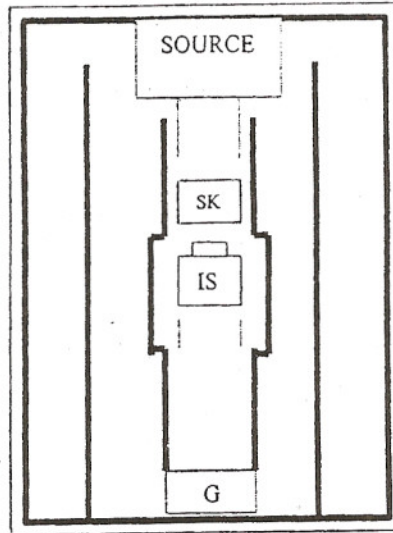




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



SK = SOURCE KELVIN IS = CURRENT SENSE

CHIP BACK IS DRAIN

Topside Metal: Al
Backside: CrNiAg
Backside Potential: -
Mask Ref: GEN 3
Bond Pads : -

APPROVED BY: CD
MFG: IR

DIE SIZE : .227" x .171"
THICKNESS: .016"

DATE: 10/7/03
P/N: IRC640

DG 10.1.2
Rev A 3-4-99